Pre Driver IC for single phase Brushless Motor

KA44171A
Datasheet

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■ IMPORTANT NOTICE

Regarding the specifications of this product, it is considered that you have agreed to the quality level and disclaimer described below.

Support for industry standards and quality standards

Functional safety standards for automobiles ISO26262	**No**
AEC-Q100	**No**
Market failure rate	**50Fit**

Disclaimer

1. When the application system is designed using this IC, please design the system at your own risk. Please read, consider, and apply appropriate usage notes and description in this standard.

2. When designing your application system, please take into the consideration of break down and failure mode occurrence and possibility in semiconductor products. Measures on the systems such as, but not limited to, redundant design, mitigating the spread of fire, or preventing glitch, are recommended in order to prevent physical injury, fire, social damages, etc. in using the Nuvoton Technology Japan Corporation (hereinafter referred to as NTCJ) products.

3. When using this IC, for each actual application systems, verify the systems and the all functionality of this IC as intended in application systems and the safety including the long-term reliability at your own risk

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5. This IC does not have any security functions using cryptographic algorithms, such as authentication, encryption, tampering detection.

6. Unless this IC is indicated by NTCJ to be used in applications as meeting the requirements of a particular industry standard (e.g., ISO 9001, IATF 16949, ISO 26262, etc.), this IC is neither designed nor intended for use in such environments for that applications. NTCJ shall not be held responsible for not meeting the requirements of a particular industry standard.

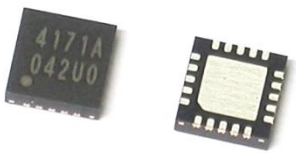
7. Using IC that have been indicated as compliant with industry functional safety standards does not warrant that the application meets the requirements of industry functional safety standards. NTCJ shall not be held responsible for the application compliance with requirements of the particular industry functional safety standard.

8. Unless this IC is indicated by NTCJ to be used in applications as meeting the requirements of a particular quality standard (e.g., AECQ-100, etc.), this IC is neither designed nor intended for use in such the environments for that applications. NTCJ shall not be held responsible for not meeting the requirements of a particular quality standard.

9. In case of damages, costs, losses, and/or liabilities incurred by NTCJ arising from customer's non-compliance with above from 1 to 8, customer will indemnify NTCJ against every damages, costs, losses and responsibility.

FEATURES

- Supply voltage range: 5.0V ~ 36 V
- Pre Driver for single phase Motor(Pch /Nch MOS FET driving)
- Phase shift function and Soft switching make high efficiency and silent driving.
- Some variable functions by A/D input (6ports 5bit) accept various applications.
  Soft switching period, Phase shift, Minimum speed, Motor lock detection / release time, Soft start time, PWM output frequency.
- FG pulse or LD (Motor lock detection) output can be selected.
- Various protection functions.
  Under voltage lock out (UVLO), Thermal protection
  Current limiter, Motor lock detection.
- Small package: QFN 20L (3x3x0.8mm3, Lead Pitch 0.4mm)



DESCRIPTION

KA44171A is Pre Driver IC for single phase Brushless Motor. it can apply DC or PWM signal for Motor speed control input.

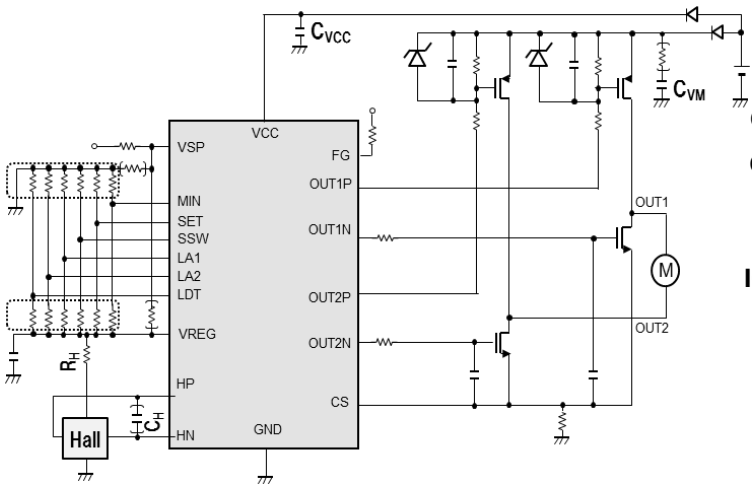
PWM soft switching function and Motor current phase setting can makes Motor current direction switch smoothly, high efficiency and silent driving.

Wide supply voltage range can use various external power MOSFET. it can drive various Motor using 12V,24,and 48V power supply.

APPLICATIONS

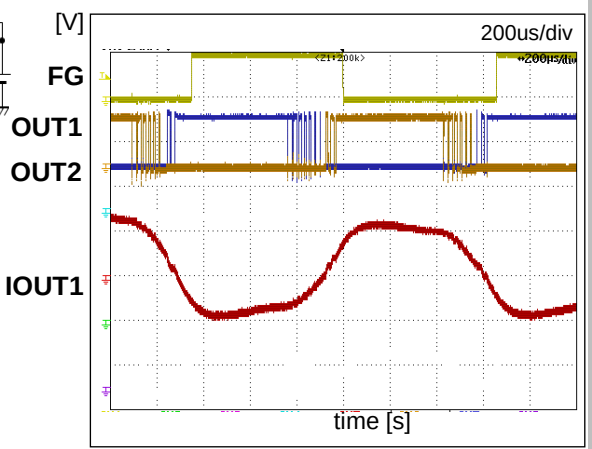
- Server, Cellular Base station,
  Factory automation, Home appliance

TYPICAL APPLICATION



Notes: The application circuit is an example. The operation of the mass production set is not guaranteed. Sufficient evaluation and verification is required in the design of the mass production set. The Customer is fully responsible for the incorporation of the above illustrated application circuit in the design of the equipment.

TYPICAL CHARACTERISTICS



Condition : V_{CC} = 12V,
PWM input duty =100%
C_{VCC} = 10µF

CONTENTS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Notes
Supply voltage	V_{CC}	–0.3 ~ +39	V	*1
Operating ambient temperature	T_{opr}	–40 ~ +105	°C	*2
Junction temperature	T_j	–40 ~ +150	°C	*2
Storage temperature	T_{stg}	–55 ~ +150	°C	*2
Input Voltage Range	V_{VSP}, V_{HP}, V_{HN}	–0.3 ~ +6	V	—
	V_{CS}	+6	V	—
	V_{MIN}, V_{SET}, V_{SSW}, V_{LA1}, V_{LA2}, V_{LDT}	–0.3 ~ V_{REG}+0.3	V	—
Input Current Range	I_{VSP}	-1 ~ +1	mA	—
Output Voltage Range	V_{FG}	–0.3 ~ +39	V	—
	V_{OUT1P}, V_{OUT2P}	+39	V	*3
	V_{OUT1N}, V_{OUT2N}	+15	V	*3
	V_{REG}	–0.3 ~ +6	V	*3
Output Current Range	I_{OUT1P}, I_{OUT1N}, I_{OUT2P}, I_{OUT2N}	–30 ~ +30	mA	*4
	I_{FG}	–1 ~ +10	mA	—
	I_{VREG}	–20 ~ 0	mA	*4
ESD	HBM	2	kV	—
	MM	200	V	—

Notes: This product may sustain permanent damage if subjected to conditions higher than the above stated absolute maximum rating. This rating is the maximum rating and device operating at this range is not guaranteed as it is higher than our stated recommended operating range. When subjected under the absolute maximum rating for a long time, the reliability of the product may be affected.

*1: The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

*2: Except for the power dissipation, operating ambient temperature, and storage temperature, all ratings are for Ta = 25℃.

*3: Applying external voltage into these pins is prohibited. Do not exceed the stated ratings even in transient state.

*4: Applying external current into these pins is prohibited. Do not exceed the stated ratings even in transient state.

POWER DISSIPATION RATING

Package	θ_{j-a}	PD (Ta=25 °C)	PD (Ta=105 °C)
QFN 20L (3x3x0.8mm3, Lead Pitch0.4mm)	83.6°C/W	1.494W	0.538W

Notes: For the actual usage, follow the power supply voltage, load and ambient temperature conditions to ensure that there is enough margin and the thermal design does not exceed the allowable value.

*1: Glass-Epoxy Substrate (2 Layers) [50 x 50 x 0.8 t](mm),
Heat dissipation fin: Die-pad, Soldered. (Heat dissipation via 2 layer board)

CAUTION

Although this IC has built-in ESD protection circuit, it may still sustain permanent damage if not handled properly. Therefore, proper ESD precautions are recommended to avoid electrostatic damage to the MOS gates.

RECOMMENDED OPERATING CONDITIONS

項 目	記 号	Min.	Typ.	Max.	単位	注
Supply voltage range	V_{CC}	5.0	—	36	V	*1
Input voltage range	V_{HP}, V_{HN}	0	—	1.5	V	*2
	V_{VSP}	0	—	5	V	*2
	V_{MIN}, V_{SET}, V_{SSW}, V_{LA1}, V_{LA2}, V_{LDT}	0	—	V_{REG}	V	*2
External constants	C_{VM}	—	10	—	µF	*3
	C_{VCC}	—	0.1	—	µF	*3
	C_{VREG}	—	0.1	—	µF	*3

Notes *1: It is a value under the conditions which do not exceed the absolute maximum rating and the power dissipation.

*2: For setting range of input control voltage, refer to Electrical Characteristics and Operation.

*3: Operation of mass production set is not guaranteed. Perform enough evaluation and verification on the design of mass production set. If the VCC terminal voltage is raised by the regenerative current, at the time of start-up or stop operating Please make countermeasure, Application information is shown at Page.27,28.

ELECTRICAL CHARACTERISTICS

V_{CC} = 12.0 V

Note: T_a = 25°C ± 2°C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Circuit current							
V_{CC} current	I_{CC}	V_{CC}= 24V	1.5	2.7	3.5	mA	—
Regulator Block							
Output voltage	V_{REG}	—	3.1	3.3	3.5	V	—
Output impedance	Z_{VREG}	I_{VREG} = –5mA	—	—	10	Ω	—
FG(LD) Block							
Low-level output voltage	V_{OLFG}	I_{FG} = 5mA	—	0.1	0.3	V	—
Output leak current	I_{LFG}	V_{FG} = 36V	—	—	5	µA	—
Hall Block							
Input dynamic range	V_{HAD}	—	0	—	1.5	V	—
Pin input current	I_{HAC}	—	–2	0	2	µA	—
Minimum input voltage amplitude	V_{HAA}	—	25	—	—	mV	—
Hysteresis width	V_{HAHYS}	—	—	10	20	mV	—
VSP speed control Block							
Low-level input current	I_{VSPL}	VSP=0V	–2	0	2	µA	—
High-level input current	I_{VSPH}	VSP=5V	25	40	55	µA	—
Stop control input voltage ratio (DC input mode)	V_{VSPMIN}	V_{MIN} = V_{REG}, VSP / V_{REG}	63	66.4	70	%	—
Maximum speed input voltage ratio (DC input mode)	V_{VSPMAX}	V_{MIN} = V_{REG}, VSP / V_{REG}	18	21.1	24	%	—
Stop control duty (PWM input mode)	D_{PWMMIN}	V_{MIN} = 0V	2	4	6	%	—
Maximum speed input duty (PWM input mode)	D_{PWMMAX}	V_{MIN} = 0V	—	100	—	%	*1*2
Low-level input voltage (PWM input mode)	V_{PWML}	V_{MIN} = 0V	—	—	0.8	V	—
High-level input voltage (PWM input mode)	V_{PWMH}	V_{MIN} = 0V	2.0	—	—	V	—
Input frequency range (PWM input mode)	F_{PWM}	V_{MIN} = 0V	15	—	60	kHz	—

Notes : *1 : These are values checked by design but not production tested.
*2 : Typical design value.

ELECTRICAL CHARACTERISTICS (continued)

V_{CC} = 12.0 V

Note: T_a = 25°C ± 2°C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Motor driving setting 5bit ADC input (MIN, SET, LDT, LA1, LA2, SSW)							
Pin input current	I_{AD}	—	–2	0	2	μA	—
5bit AD input range	V_{ADD}	—	0	—	V_{REG}	V	*1
DNL	V_{DNL}	—	-1.0	0.0	1.0	LSB	—
INL	V_{INL}	—	-1.0	0.0	1.0	LSB	—
Motor Lock Protection							
Lock detection time	t_{LOCK1}	—	0.75	1.0	1.25	s	*2
Lock release time	t_{LOCK2}	—	7.5	10.0	12.5		
Lock protection time ratio	L_{RATIO}	$L_{RATIO} = t_{LOCK2} / t_{LOCK1}$	9.5	10	10.5	—	
Soft start Block							
Soft start time	t_{SS}	—	0.6	0.8	1.0	s	*3

Notes : *1 : Each ADC setting is shown at ADC control mode table (Page.12~14).
*2 : This ADC setting value is shown at ADC control mode table (Page.12).
*3 : This ADC setting value is shown at ADC control mode table (Page.13).

ELECTRICAL CHARACTERISTICS (continued)

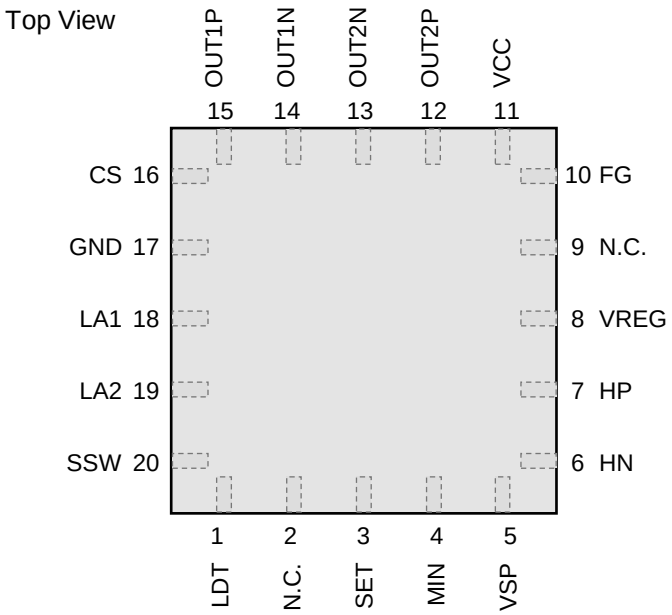
V_{CC} = 12.0 V

Note: T_a = 25°C ± 2°C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
External FET gate drive output							
Upper FET gate drive “Low” output current	I_{OUTPL}	V_O = 24V, V_{CC}=24V	12.7	17	21.3	mA	—
Upper FET gate drive “Low” output voltage	V_{OUTPL}	I_O = 5mA, V_{CC}=24V	—	0.3	0.5	V	—
Upper FET gate drive “High” output voltage	V_{OUTPH}	I_O = –5mA, V_{CC}=24V	V_{CC} –0.6	V_{CC} –0.35	—	V	—
Lower FET gate drive “Low” output voltage	V_{OUTNL}	I_O = 5mA, V_{CC}=24V	—	0.3	0.5	V	—
Lower FET gate drive “High” output voltage	V_{OUTNH}	I_O = –5mA, V_{CC}=24V	8.5	10.5	12.5	V	—
Lower FET gate drive “High” output voltage (Vcc=5V)	V_{OUTNHL}	I_O = –5mA, V_{CC}=5V	V_{CC} –2.0	V_{CC} –1.0	V_{CC} –0.5	V	—
PWM output frequency 1	F_{PWMDO1}	V_{SET} = V_{REG}	30	40	50	kHz	*1
PWM output frequency 2	F_{PWMDO2}	V_{SET} = 0 V	22.5	30	37.5		
Thermal protection							
Protection operating temperature	TSD_{ON}	—	—	160	—	°C	*2*3
Hysteresis width	TSD_{HYS}	—	—	25	—	°C	*2*3
Under voltage lock out							
Protection operating voltage	V_{LVON}	—	—	3.5	—	V	*2*3
Hysteresis width	V_{LVOHYS}	—	—	0.2	—	V	*2*3
Motor current limiter							
Detection voltage 1	V_{CS1}	Normal driving mode	135	150	165	mV	—
Detection voltage 2	V_{CS2}	Start-up driving mode	70	90	110	mV	—

Notes : *1: This ADC setting value is shown at ADC control mode table (Page.13).
*2 : Typical design value.
*3 : These are values checked by design but not production tested.

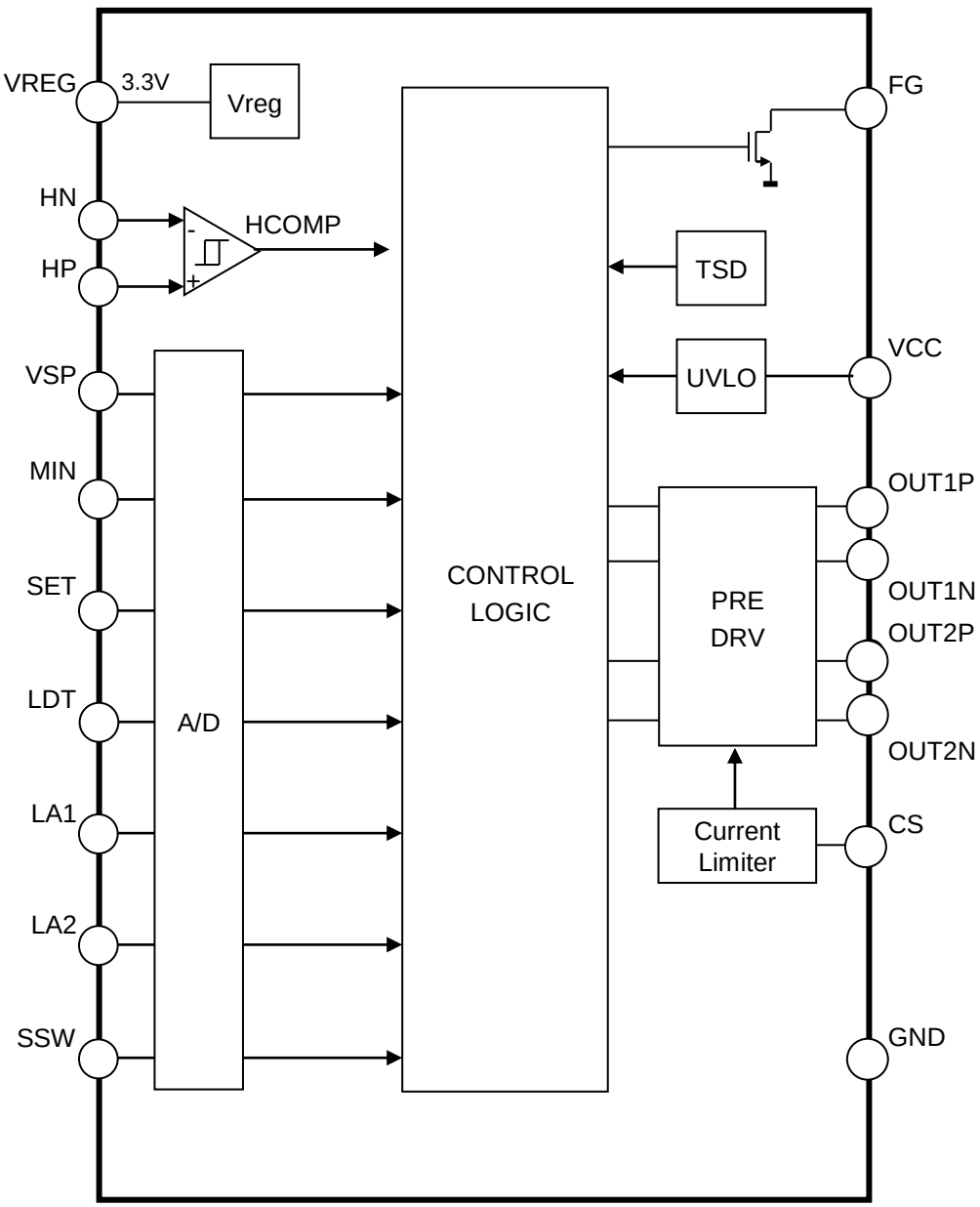
PIN CONFIGURATION



PIN FUNCTIONS

Pin No.	端子名	Type	説明
1	LDT	Input	ADC input. Motor lock protection setting. FG or LD output setting.
2	N.C.	—	—
3	SET	Input	ADC input. Soft start time setting. PWM output frequency setting.
4	MIN	Input	ADC input. Minimum speed setting. VSP input mode setting.
5	VSP	Input	Motor speed control input.
6	HN	Input	Hall amplifier input (-).
7	HP	Input	Hall amplifier input (+).
8	VREG	Output	Internal reference voltage.
9	N.C.	—	—
10	FG	Output	FG or LD output.
11	VCC	Power	Power supply voltage input.
12	OUT2P	Output	OUT2 Upper FET gate drive output.
13	OUT2N	Output	OUT2 Lower FET gate drive output.
14	OUT1N	Output	OUT1 Upper FET gate drive output.
15	OUT1P	Output	OUT1 Lower FET gate drive output.
16	CS	Input	Motor current detection input.
17	GND	Ground	Ground.
18	LA1	Input	ADC input. VSP reference setting at Motor drive phase shift operating.
19	LA2	Input	ADC input. Maximum Motor drive phase shift setting.
20	SSW	Input	ADC input. Soft switching period setting.

BLOCK DIAGRAM



Notes: This block diagram is for explaining functions. Part of the block diagram may be omitted, or it may be simplified.

OPERATION

Note) The characteristics listed below are reference values derived from design of the IC and are not guaranteed.

■ADC control mode table (V_{REG}=3.3V)

Step	LDT(1)				
	ADC Input voltage [V] A=V_{REG}/32 (Value at V_{REG}=3.3V)	FG(10) pin output signal	Motor lock detection time [s]	Motor lock protection release time [s]	Motor lock protection time ratio
31	32 × A (3.3V)	LD	off	off	–
30					
29	29 × A (2.991V)		1.0	10	1:10
28					
27	27 × A (2.783V)		0.5	5.0	1:10
26					
25	25 × A (2.578V)		0.3	3.0	1:10
24					
23	23 × A (2.371V)		0.3	4.5	1:15
22					
21	21 × A (2.166V)		0.5	7.5	1:15
20					
19	19 × A (1.959V)		0.5	10	1:20
18					
17	17 × A (1.753V)		0.3	6.0	1:20
16					
15	15 × A (1.547V)	FG	off	off	–
14					
13	13 × A (1.341V)		1.0	10	1:10
12					
11	11 × A (1.134V)		0.5	5.0	1:10
10					
9	9 × A (0.928V)		0.3	3.0	1:10
8					
7	7 × A (0.722V)		0.3	4.5	1:15
6					
5	5 × A (0.516V)		0.5	7.5	1:15
4					
3	3 × A (0.309V)		0.5	10	1:20
2					
1	0		0.3	6.0	1:20
0					

OPERATION(continued)

Note) The characteristics listed below are reference values derived from design of the IC and are not guaranteed.

■ADC control mode table (V_{REG}=3.3V)

Step	SET (3)			MIN (4)		
	ADC input voltage [V] A=V_{REG}/64 (Value at V_{REG}=3.3V)	PWM output frequency [kHz]	Soft start time [s]	ADC input voltage [V] A=V_{REG}/64 (Value at V_{REG}=3.3V)	VSP input mode	Min duty [%] (*2)
31	64 × A (3.3V)	40	OFF	64 × A (3.3V)	DC input mode	44.1
30	61 × A (3.145V)		0.8	61 × A (3.145V)		40.9
29	59 × A (3.042V)		1.6	59 × A (3.042V)		37.8
28	57 × A (2.939V)		2.4	57 × A (2.939V)		34.7
27	55 × A (2.836V)		3.2	55 × A (2.836V)		31.5
26	53 × A (2.733V)		4.0	53 × A (2.733V)		28.4
25	51 × A (2.630V)		4.8	51 × A (2.630V)		25.2
24	49 × A (2.527V)		5.6	49 × A (2.527V)		22.1
23	47 × A (2.423V)		6.4	47 × A (2.423V)		18.9
22	45 × A (2.320V)		7.2	45 × A (2.320V)		15.8
21	43 × A (2.217V)		8.0	43 × A (2.217V)		12.6
20	41 × A (2.114V)		8.8	41 × A (2.114V)		9.5
19	39 × A (2.011V)		9.6	39 × A (2.011V)		6.3
18	37 × A (1.908V)		10.4	37 × A (1.908V)		3.2
17	35 × A (1.805V)		11.2	34 × A (1.753V)		0.0
16	33 × A (1.702V)		Do not set *1 (12.0)			
15	31 × A (1.598V)	30	Do not set *1 (12.0)	31 × A (1.598V)	PWM input mode	(44.1) (*1)
14	29 × A (1.495V)		11.2	29 × A (1.495V)		40.9
13	27 × A (1.392V)		10.4	27 × A (1.392V)		37.8
12	25 × A (1.289V)		9.6	25 × A (1.289V)		34.7
11	23 × A (1.186V)		8.8	23 × A (1.186V)		31.5
10	21 × A (1.083V)		8.0	21 × A (1.083V)		28.4
9	19 × A (0.980V)		7.2	19 × A (0.980V)		25.2
8	17 × A (0.877V)		6.4	17 × A (0.877V)		22.1
7	15 × A (0.773V)		5.6	15 × A (0.773V)		18.9
6	13 × A (0.670V)		4.8	13 × A (0.670V)		15.8
5	11 × A (0.567V)		4.0	11 × A (0.567V)		12.6
4	9 × A (0.464V)		3.2	9 × A (0.464V)		9.5
3	7 × A (0.361V)		2.4	7 × A (0.361V)		6.3
2	5 × A (0.258V)		1.6	5 × A (0.258V)		3.2
1	3 × A (0.155V)		0.8	0		0.0
0	0		OFF			

*1: Step.15 and Step.16 are very different set value.
Please avoid to set Sep.15 or Step.16, because set value may be changed by ADC voltage shifted unintentionally.
each value is set ( ) at Step.15 or Step.16.

*2: Switching response may be delayed by external parts. it causes that Min duty is changed.
The Min duty in above table means design value at Vcc=12V and OUT1P (OUT2P) pin is open.

OPERATION(continued)

Note) The characteristics listed below are reference values derived from design of the IC and are not guaranteed.

■ADC control mode table (V_{REG}=3.3V)

Step	ADC input voltage [V] A=V_{REG}/64 (Value at V_{REG}=3.3V)	LA1 (18) *3	LA2 (19) *3	SSW (20)	
		VSP ratio at Motor drive phase shift operation. [%] *2	Maximum motor drive phase shift. [deg]	Soft switching period. [deg]	
				Rise	Fall
31	64 × A (3.3V)	Do not set *1	84.4	22.5	90.0
30	61 × A (3.145V)		81.6		87.2
29	59 × A (3.042V)	90.6	78.8		84.4
28	57 × A (2.939V)	87.5	75.9		81.6
27	55 × A (2.836V)	84.4	73.1	19.7	78.8
26	53 × A (2.733V)	81.3	70.3		75.9
25	51 × A (2.630V)	78.1	67.5		73.1
24	49 × A (2.527V)	75.0	64.7		70.3
23	47 × A (2.423V)	71.9	61.9	16.9	67.5
22	45 × A (2.320V)	68.8	59.1		64.7
21	43 × A (2.217V)	65.6	56.3		61.9
20	41 × A (2.114V)	62.5	53.4		59.1
19	39 × A (2.011V)	59.4	50.6	14.1	56.3
18	37 × A (1.908V)	56.3	47.8		53.4
17	35 × A (1.805V)	53.1	45.0		50.6
16	33 × A (1.702V)	50.0	42.2		47.8
15	31 × A (1.598V)	46.9	39.4	11.3	45.0
14	29 × A (1.495V)	43.8	36.6		42.2
13	27 × A (1.392V)	40.6	33.8		39.4
12	25 × A (1.289V)	37.5	30.9		36.6
11	23 × A (1.186V)	34.4	28.1	8.4	33.8
10	21 × A (1.083V)	31.3	25.3		30.9
9	19 × A (0.980V)	28.1	22.5		28.1
8	17 × A (0.877V)	25.0	19.7		25.3
7	15 × A (0.773V)	21.9	16.9	5.6	22.5
6	13 × A (0.670V)	18.8	14.1		19.7
5	11 × A (0.567V)	15.6	11.3		16.9
4	9 × A (0.464V)	12.5	8.4		14.1
3	7 × A (0.361V)	9.4	5.6	2.8	11.3
2	5 × A (0.258V)	6.3	2.8		8.4
1	3 × A (0.155V)	3.1	0.0		5.6
0	0	0	0.0		2.8

*1: The value at Step.30 and 31 is not exact. but even if they are set, IC is not destroyed.
*2 : This value means VSP ratio. 0[%] means VSP stop control input, and 100[%] means VSP Maximum speed input.
*3 : When both LA1 and LA2 are set higher, Their real value have a little error from set value. Perform evaluation and verification enough.

OPERATION(continued)

Note) The characteristics listed below are reference values derived from design of the IC and are not guaranteed.

■Start up

When VCC voltage within operation range us input, IC drives motor at startup mode and shifted to normal mode.

■Start up mode / Normal mode

Driving mode which is selected by continuous detection. during driving the motor.
At motor accelerating : When Motor speed > 6.67Hz as FG frequency,
Motor drive mode become from Startup mode to Normal mode.
At motor slowdown : When Motor speed < 6.67Hz as FG frequency,
Motor drive mode become from Normal mode to Start up mode.

・Start up mode
Motor drive phase shift is set 0 deg
Soft switching period is set 0 deg.
Motor current limit detection is set 90mV (Vcs2).

・Normal mode
Motor drive phase shift is set by ADC input.
Soft switching period is set by ADC input.
Motor current limit detection is set 150mV (Vcs1).

【 At motor accelerating 】

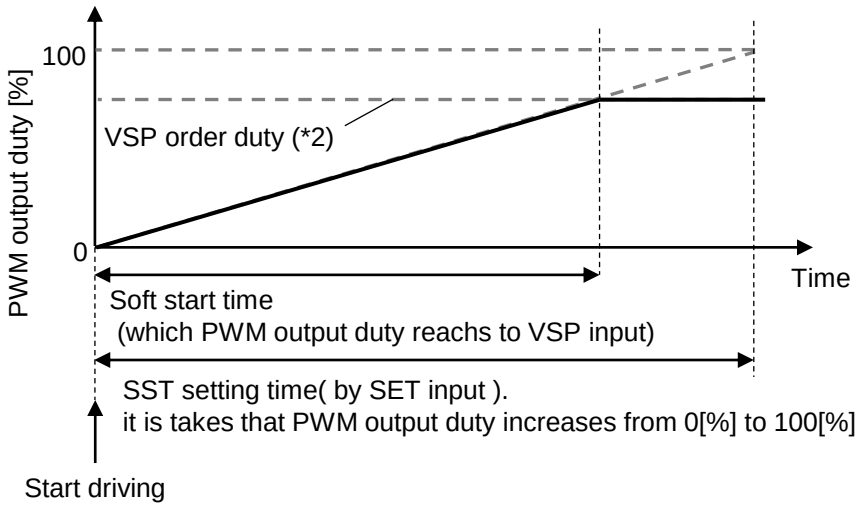
FG signal	FG frequency < 6.67Hz	FG frequency > 6.67Hz
Drive mode	**Start up mode** Motor drive phase shift : 0deg Soft switching period : 0deg Motor current limit detection : 90mV	**Normal mode** Motor drive phase shift : ADC setting Soft switching period : ADC setting Motor current limit detection : 150mV

OPERATION(continued)

Note) The characteristics listed below are reference values derived from design of the IC and are not guaranteed.

■Soft start (SST)

Soft start (SST) is set by SET pin input voltage (*1).
Relation of Soft start time setting, VSP setting and PWM output duty is shown at below.



・Precaution for Soft start function.
When soft start is active, Motor current increase slowly from start up.
if soft start time is set too long, Motor current at start up is little. and torque is lack and Motor keeps stop. then, when FG is not detected during Motor lock detection time, Motor lock protection works.

Notes : *1 : This ADC setting value is shown at ADC control mode table (Page.13).
*2 : This value means VSP ratio. 0[%] means VSP stop control input, and 100[%] means VSP Maximum speed input.

OPERATION(continued)

Note) The characteristics listed below are reference values derived from design of the IC and are not guaranteed.

■PWM output frequency

External FET is driven for PWM switching.
PWM output frequency is set by SET pin input voltage (*1).

SET input and PWM output frequency
Step. 0 ~ 14 : 30kHz (typ)
Step.17 ~ 31 : 40kHz (typ)

Notes : *1 : This ADC setting value is shown at ADC control mode table (Page.13).

■Speed control

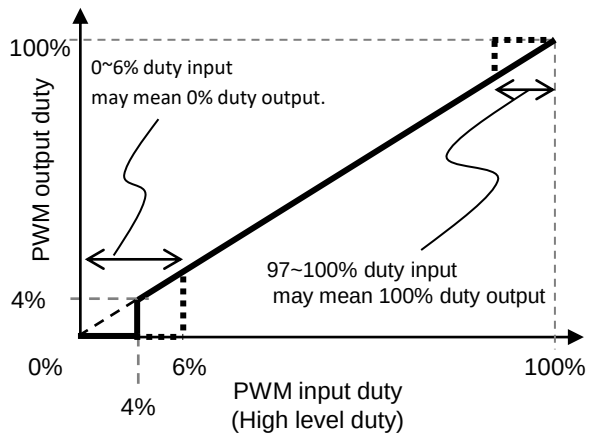
Speed control input can be selected from PWM or DC mode. it is set by MIN pin input voltage.

MIN input voltage = Step. 0~14 : PWM input mode.
MIN input voltage = Step.16 ~31 : DC input mode

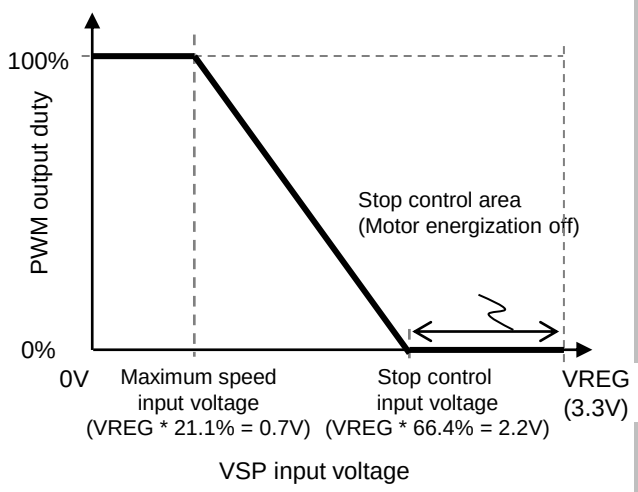
(1) PWM input mode
- VSP pin is input PWM signal.
  Motor current is driven by PWM switching.
- PWM input duty means PWM output duty.
  but, 0~6% duty input may mean 0% duty output.
  97~100% duty input may mean 100% duty output.

(2) DC input mode
- VSP pin is input DC voltage.
  VSP input voltage means PWM output duty.

(1) PWM input mode



(2) DC input mode



OPERATION(continued)

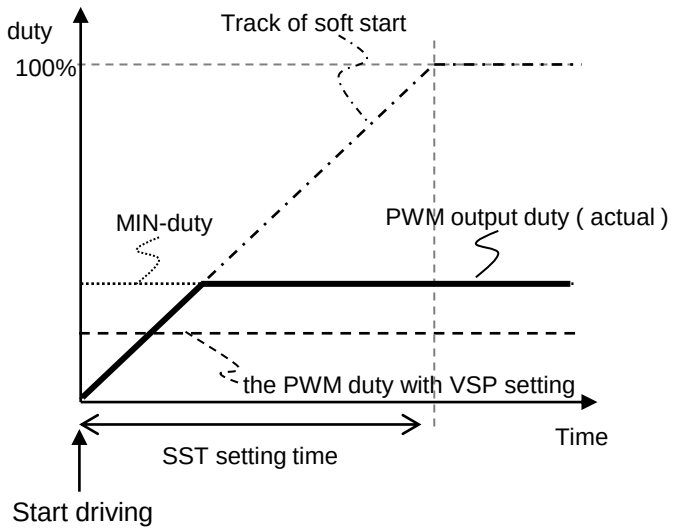
Note) The characteristics listed below are reference values derived from design of the IC and are not guaranteed.

■Min duty

When the PWM duty with VSP setting is less than Min duty with MIN pin setting.
PWM output duty becomes Min duty (*1).

At Soft start driving, PWM output duty increase from 0% duty in spite of Min duty setting.

【Start up action at MIN-duty > Speed control input】



Notes : *1 : This ADC setting value is shown at ADC control mode table (Page.13).

OPERATION(continued)

Note) The characteristics listed below are reference values derived from design of the IC and are not guaranteed.

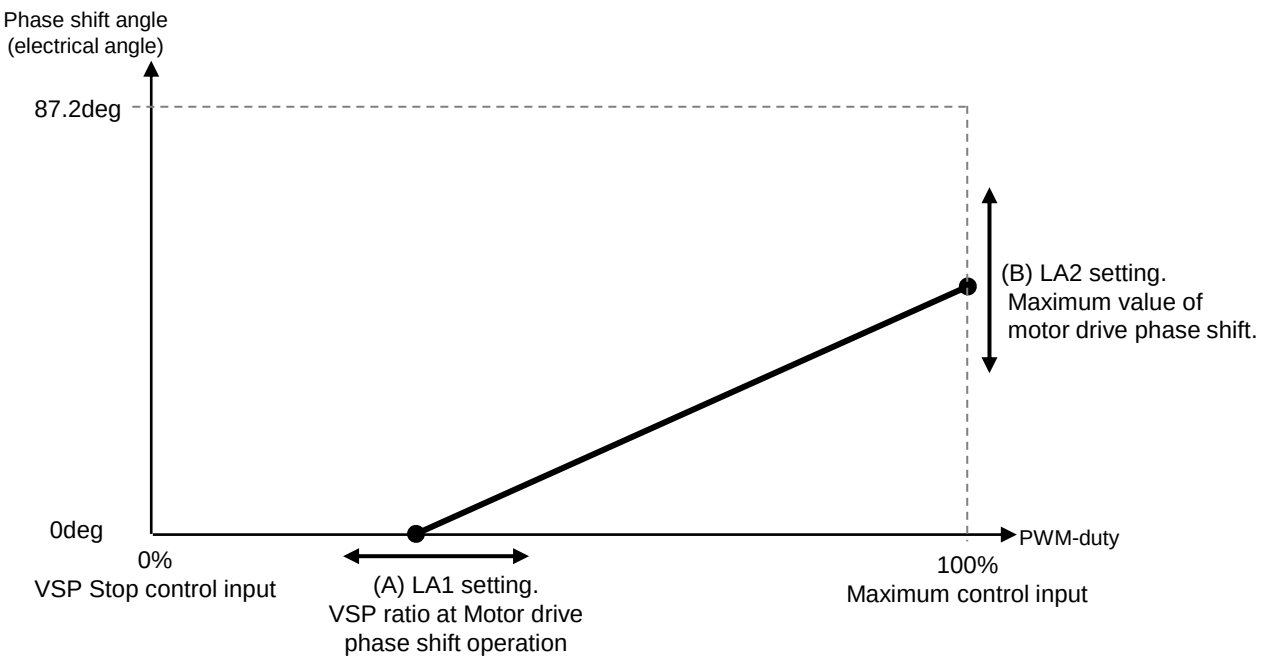
■Driving phase shift

Driving phase shift area In VSP input range, and Maximum value of motor drive phase shift, are set by LA1 and LA2 input voltage .

(A) LA1 operates VSP ratio at Motor drive phase shift operation.
this ratio means that 0[%] is Stop control input, and 100[%] is Maximum speed input.
When VSP input is more than the value of this ratio, Motor drive phase shift is operating.

(B) LA2 operates Maximum value of motor drive phase shift at VSP 100[%] input.

Driving phase shift works as below diagram.



*1 : This ADC setting value is shown at ADC control mode table (Page.14).
*2 : When both LA1 and LA2 are set higher, Their real value have a little error from set value.
Perform evaluation and verification enough.

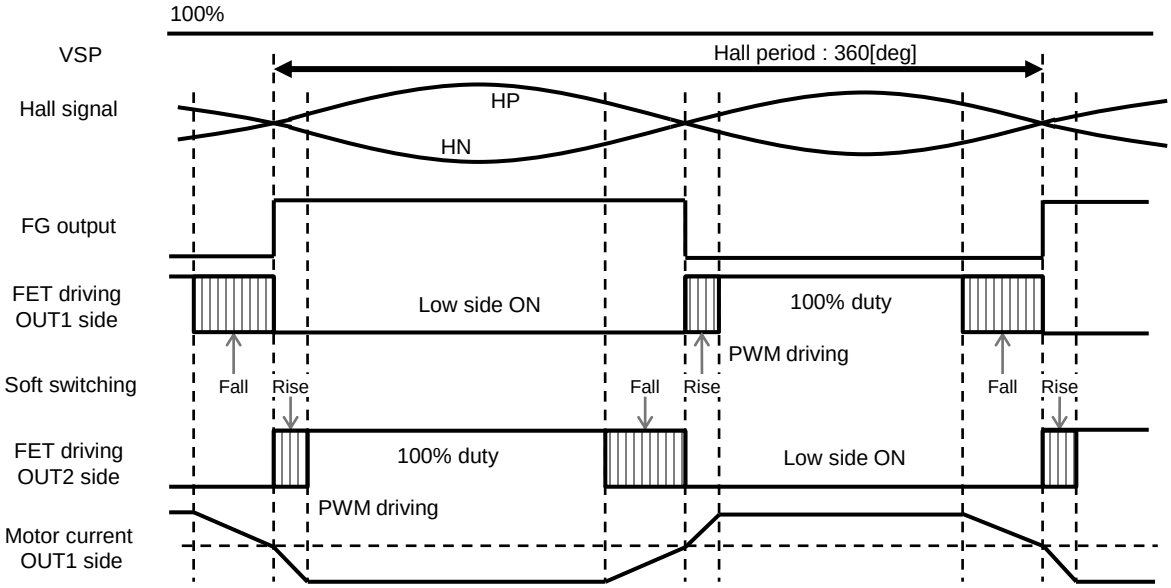
OPERATION(continued)

Note) The characteristics listed below are reference values derived from design of the IC and are not guaranteed.

■Soft switching

Soft switching period is set by SSW pin input voltage.
the value of Soft switching is shown as electrical degree, Hall period is 360[deg].

At Driving phase shift : 0deg setting

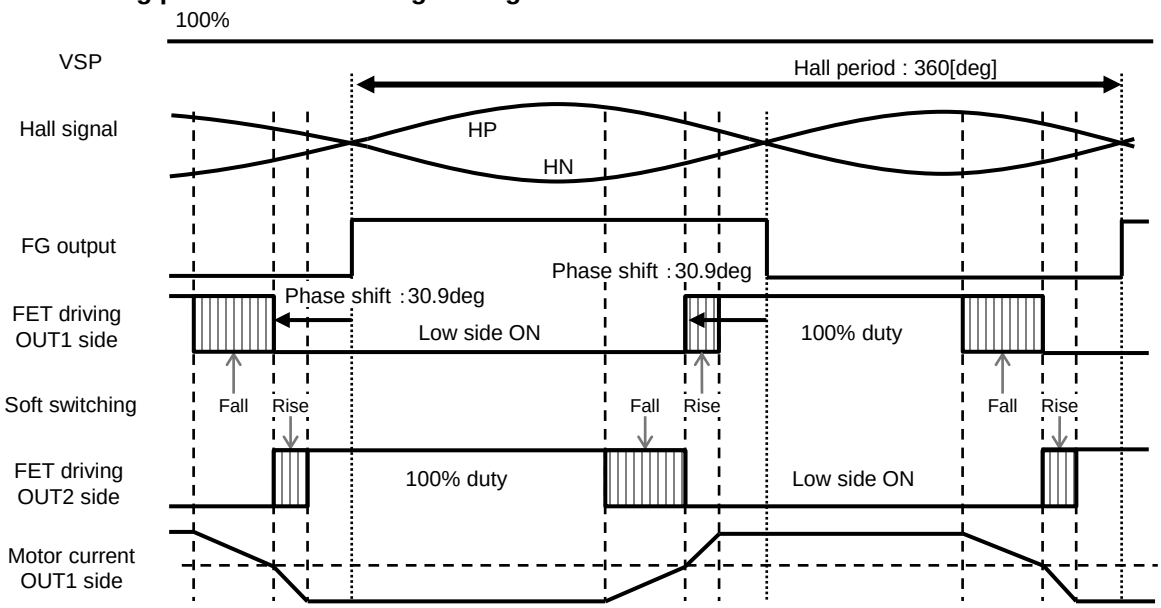


*1 : This ADC setting value is shown at ADC control mode table (Page.14).

■Driving phase shift and Soft switching

Motor driving phase shift makes Motor driving phase is shifted from Hall signal.
then, Soft switching period keep applying SSW setting value.

At Driving phase shift : 30.9deg setting

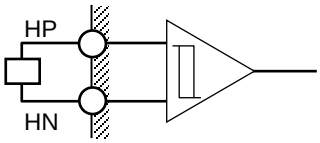


OPERATION(continued)

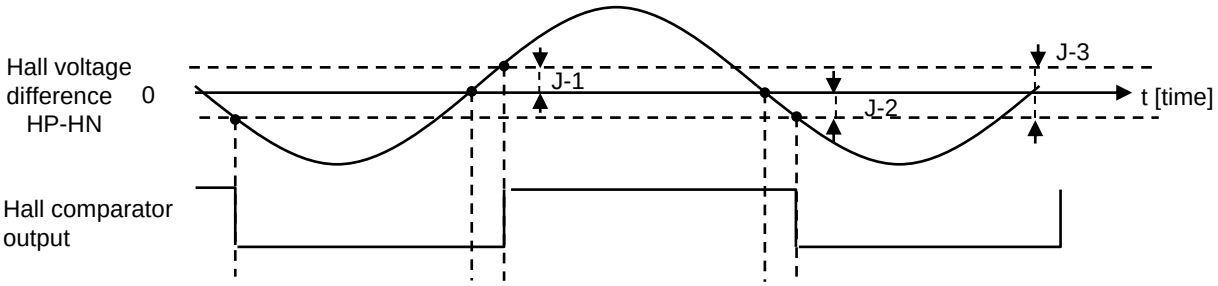
Note) The characteristics listed below are reference values derived from design of the IC and are not guaranteed.

■ Hall input

Hall hysteresis comparator carries out position detection. If the amplitude of the sine wave is small, the phase delay of the comparator output becomes significant, therefore, increase the amplitude. Recommendation is 100 mV or more. Also, if the hole chattering occurs, put capacitor between HP (7 pin) and HN (6 pin).

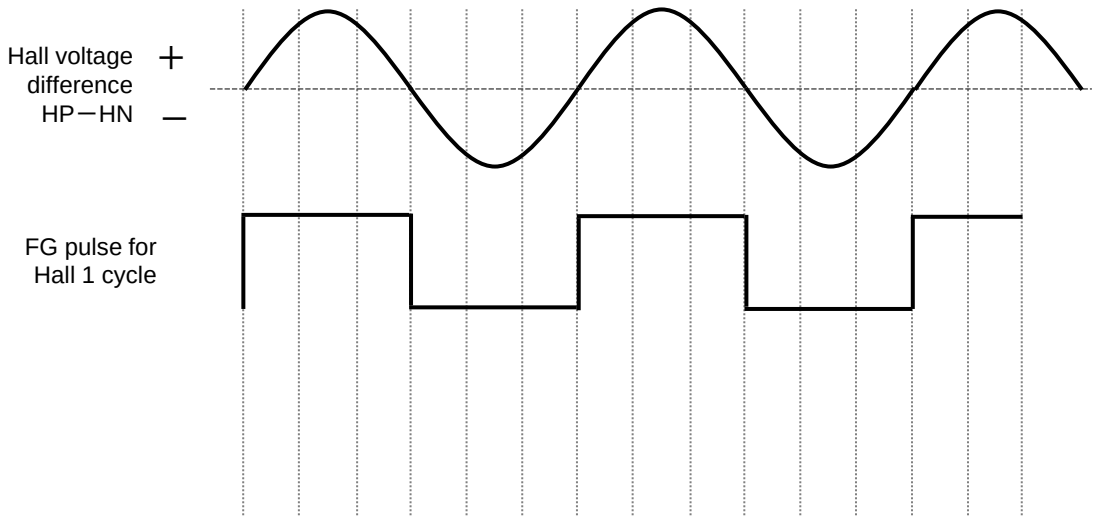


The following is a schematic diagram of the characteristics.
J-1 hysteresis level: 5 mV L → H
J-2 hysteresis level: 5 mV H → L
J-3 hysteresis width: 10 mV (typ)



・Relationship between Hall voltage and FG

For the one cycle sine wave of Hall, it outputs FG pulse one cycle.



OPERATION(continued)

Note) The characteristics listed below are reference values derived from design of the IC and are not guaranteed.

■Truth table

Condition					Output					
UVLO	TSD	Motor lock protection	VSP (*1)	HP,HN	FG (*2)	LD (*2)	OUT 1P (*3)	OUT 1N (*3)	OUT 2P (*3)	OUT 2N (*3)
Active	–	–	–	–	–	–	H	L	H	L
Mute	Mute	Active	–	HP>HN	OFF	OFF	H	H	H	L
Mute	Mute	Active	–	HP<HN	L	OFF	H	L	H	H
Mute	Active	Mute	–	HP>HN	OFF	L	H	H	H	L
Mute	Active	Mute	–	HP<HN	L	L	H	L	H	H
Mute	Mute	Mute	Stop control	HP>HN	OFF	L	H	H	H	L
Mute	Mute	Mute	Stop control	HP<HN	L	L	H	L	H	H
Mute	Mute	Mute	Drive control	HP>HN	OFF	L	H	H	H / -17mA (*4)	L
Mute	Mute	Mute	Drive control	HP<HN	L	L	H / -17mA (*4)	L	H	H

*1 : (At DC input mode) Stop control : VSP > 2.2V, Drive control : VSP<2.2 (at VREG=3.3V).
(At PWM input mode) Stop control : VSP High duty < 4%, Drive control : VSP High duty > 6%.
*2 : Either FG or LD signal is output to FG pin.
*3 : At Driving phase shift is set 0 [deg].
*4 : External FET (Pch) is driven as PWM. -17mA means 17mA sink current output.

■Protection function

Function (detector)	Operate	Release	Note
Under voltage lock out (VCC pin voltage)	3.5V	3.7V	When Vcc is less than UVLO threshold voltage. Motor energization off
Thermal shut down （Junction temperature）	160℃	135℃	When TSD is active. Motor energization off
Motor current limit (CS pin voltage）	・At Start up mode >90mV ・At Normal mode >150mV	・At start up mode <90mV ・At Normal mode <150mV	When CS voltage more than threshold voltage. Motor energization off
Motor lock protection (FG)	When FG pulse does not change within Motor lock detection time.	・at UVLO ・Reinput of VSP ・After Motor lock protection release time progress	・When Motor lock protection is active. Motor energization off ・After Motor lock protection release time progress. Protection is released. ・Motor lock detection time, and Motor lock protection release time are set by LDT pin voltage. (page .11)

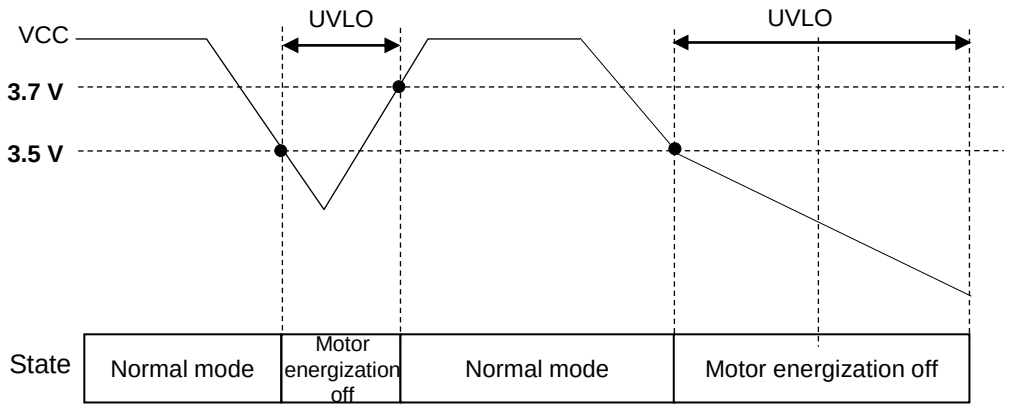
OPERATION(continued)

Note) The characteristics listed below are reference values derived from design of the IC and are not guaranteed.

■Under voltage lock out (UVLO)

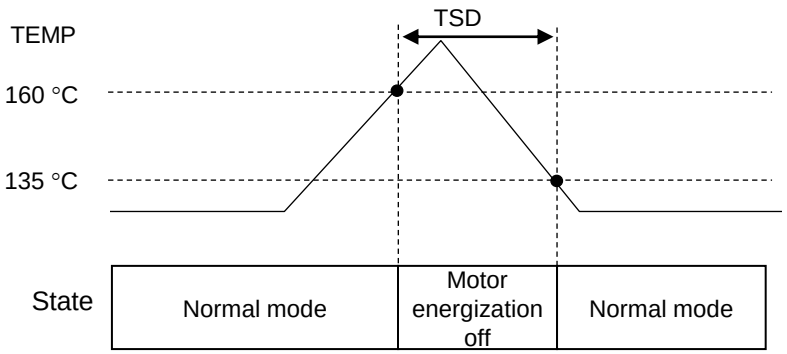
This IC monitors the voltage VCC. If VCC voltage becomes 3.5V or less, low-voltage protection is activated.
In the low voltage protection operation, all FET are OFF.

Hysteresis of 0.2V is set in the VCC low voltage protection function. If the VCC is restored to 3.7V from protection mode, the low voltage protection is released.



■Thermal shutdown (TSD)

If an IC junction temperature is 160℃ (design target value) or more, the thermal protection is activated, Motor energization gets off.
If the IC junction temperature is 135℃ (design target value) or less, the protection is released.



OPERATION(continued)

Note) The characteristics listed below are reference values derived from design of the IC and are not guaranteed.

■Motor lock protection

When FG non-signal state continues for motor lock detection time in the motor normal operation mode, locked protection circuit operates(*1).

In the locked protection mode, PWM OFF drive.
- Motor energization off
- LD = H

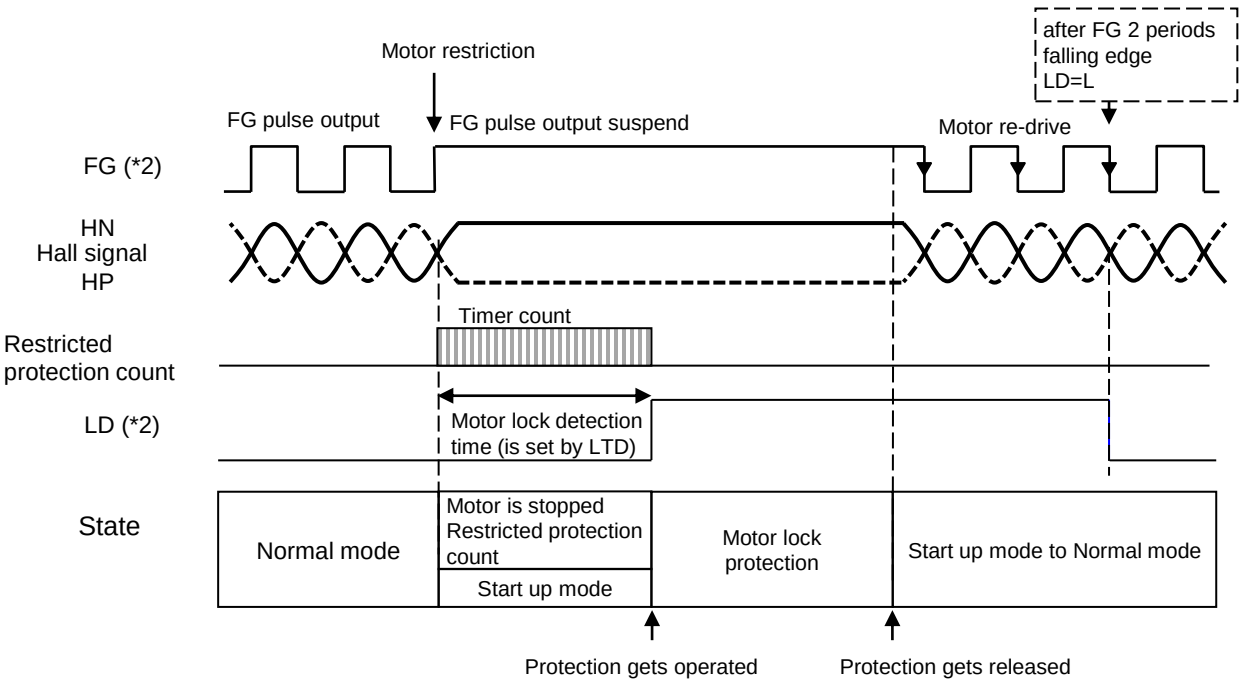
after locked protection time is passed, Motor driving is restart.
LD signal is L after FG 2 periods falling edge.

The locked protection time and the LD signal output is set by LDT pin voltage.

When the locked protection time is set OFF, the motor lock protection is not active.
When LDT is set Step.16 ~ 31, LD signal is output to FG pin.

Conditions to release the motor restricted protection, and to reset the counter are as follows.
- ・In detecting UVLO mode
- ・After Locked protection time progress
- ・VSP is input again.

Motor lock protection



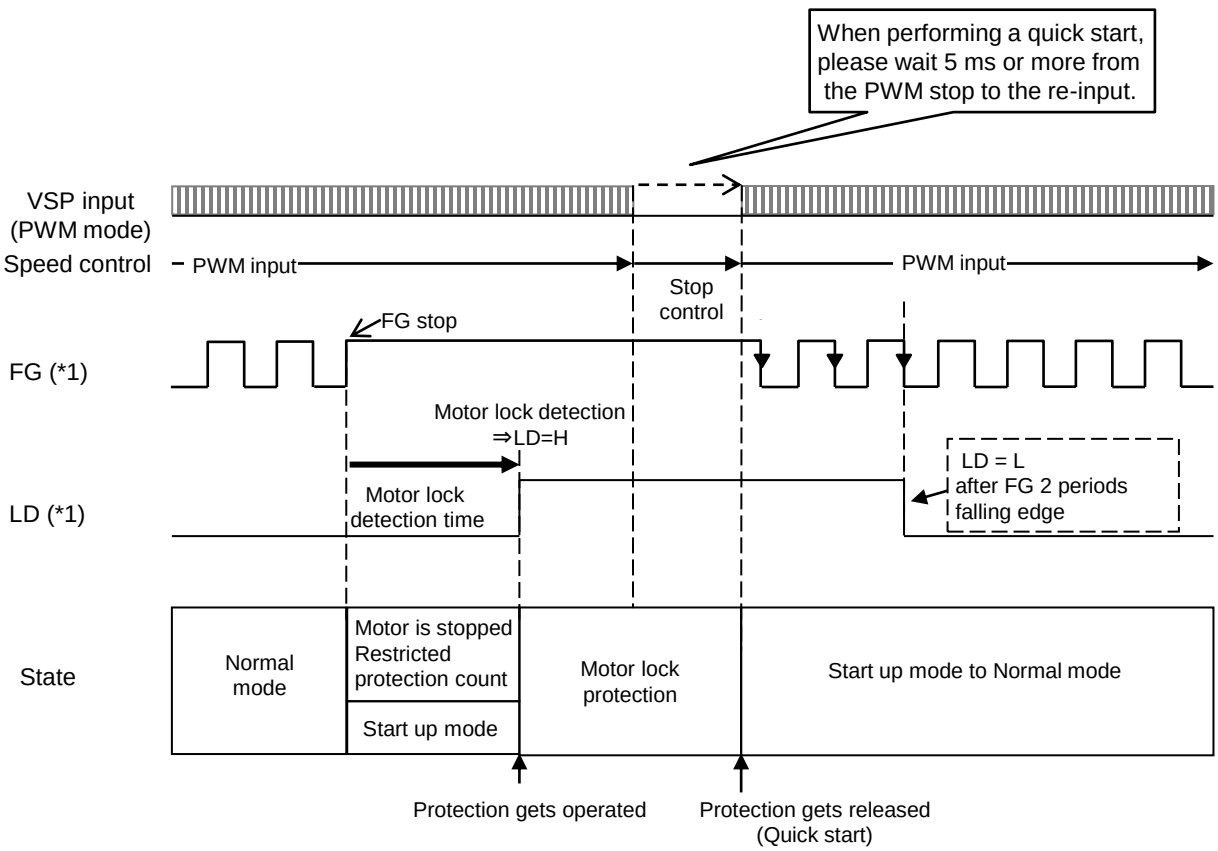
*1: This ADC setting value is shown at ADC control mode table (Page.11).
*2: Either FG or LD signal is output to FG pin.

OPERATION(continued)

Note) The characteristics listed below are reference values derived from design of the IC and are not guaranteed.

■Quick start (Motor lock protection)

By inputting the PWMI stop signal before automatic release during Motor locked protection,
and re-inputting the PWM signal,
You can release the Motor locked protection state and perform a quick start to restart the motor.
※When performing a quick start, please wait 5 ms or more from the PWM stop to the re-input.



*1: Either FG or LD signal is output to FG pin.

OPERATION(continued)

Note) The characteristics listed below are reference values derived from design of the IC and are not guaranteed.

■Current limit

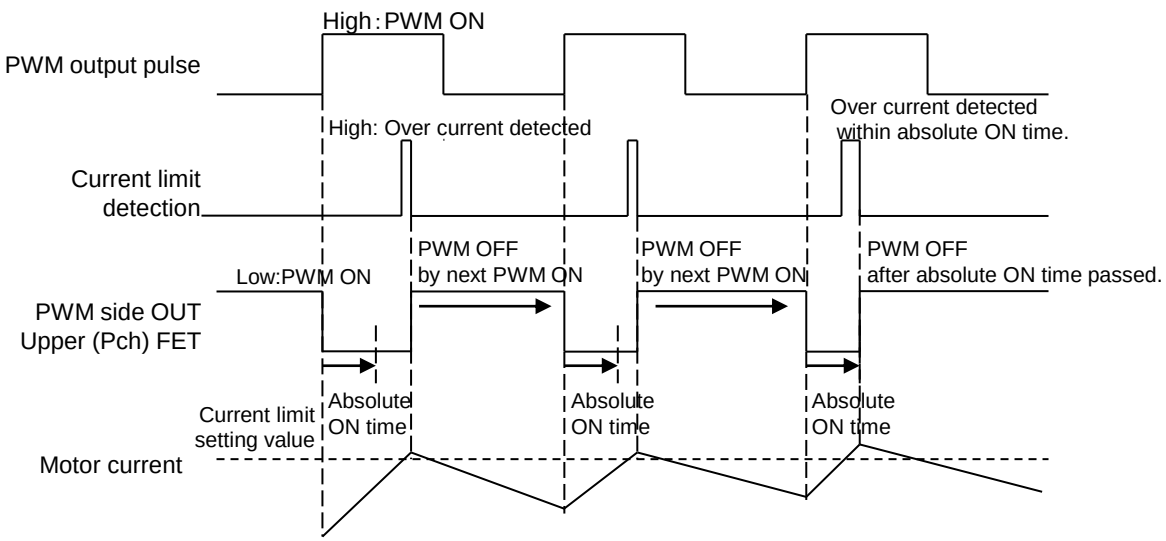
Describes the current limit protection setting at motor drive.
Motor current is detected by shunt resistance RCS.
the voltage of RCS is input to CS pin.
the value of Current limit is set by Current limit protection setting voltage and RCS resistance value.

Current limit setting value (A) = Current limit protection setting voltage (V) / RCS resistance value (Ω)

Current limit setting voltage is binary switched.
It is 150mV at normal mode and 90mV at start up mode.

When Current limit is detected, FET at PWM side OUT is OFF.
it means Motor current decreasing.
after that, this (upper) FET is ON at next PWM output pulse (PWM frequency 30kHz or 40kHz).

Current limit detection has absolute ON time 4us at switching FET from OFF to ON.
Even if CS voltage is more than Current limit protection setting voltage within absolute ON time, PWM is not OFF for this time.

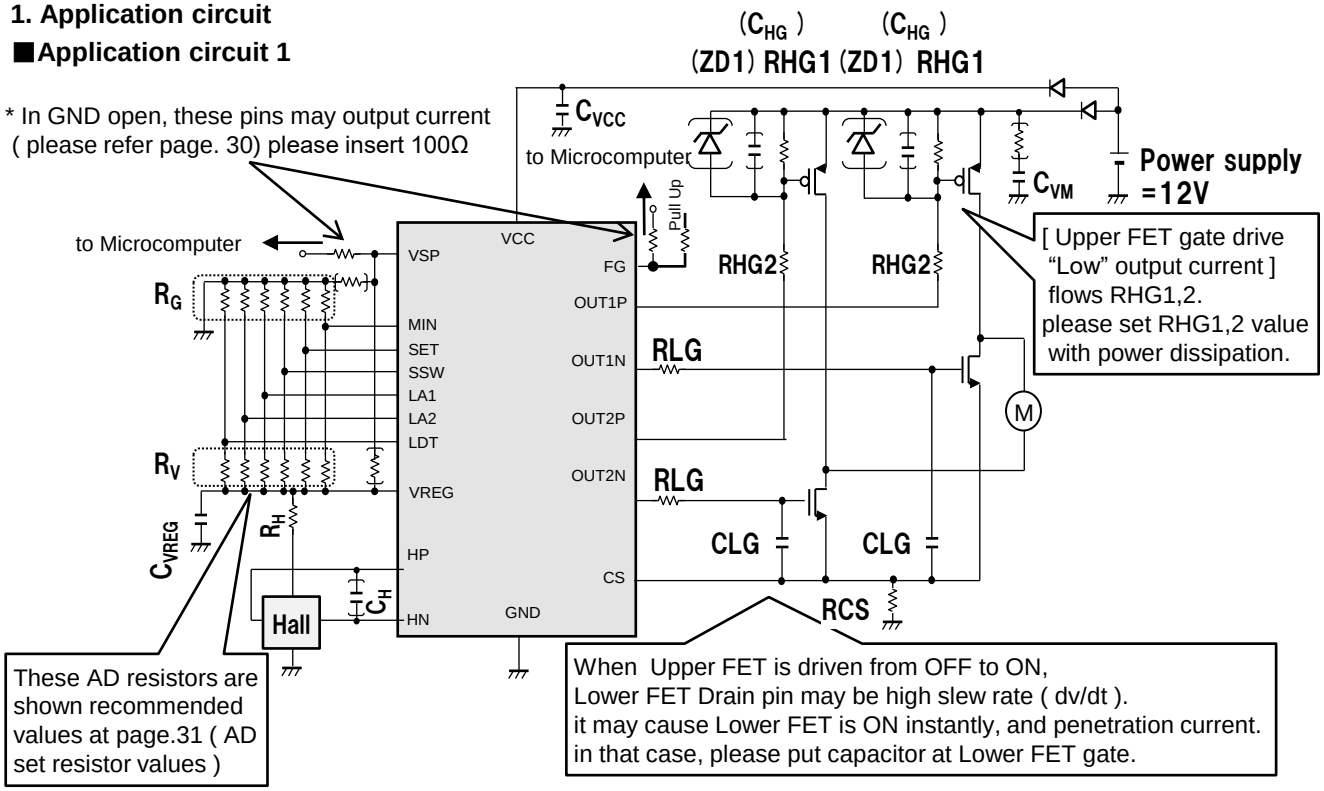


Normal mode(Motor speed > FG frequency 6.67Hz) : Current limit setting voltage = 150mV (Vcs1)
Start up mode(Motor speed < FG frequency 6.67Hz) : Current limit setting voltage = 90mV (Vcs2)

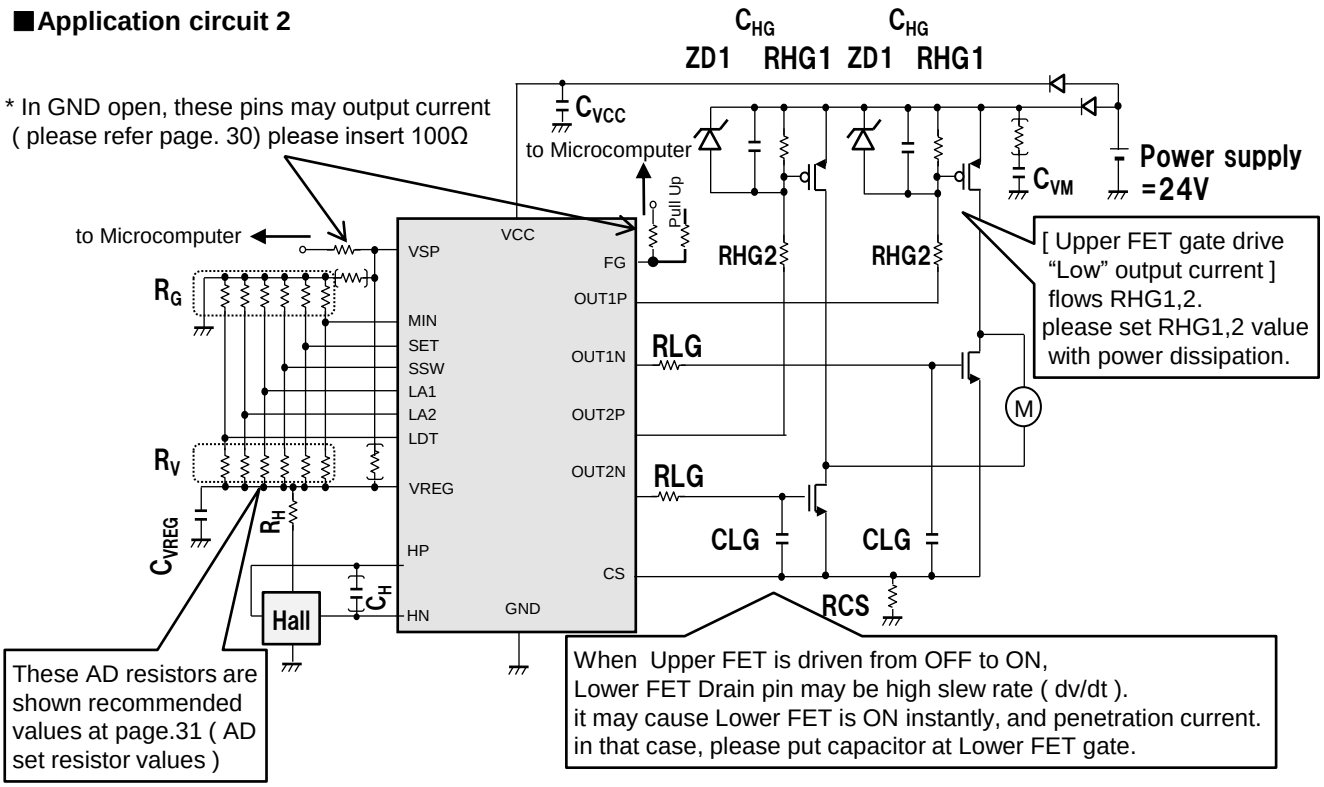
APPLICATION INFORMATION

1. Application circuit

■Application circuit 1



■Application circuit 2

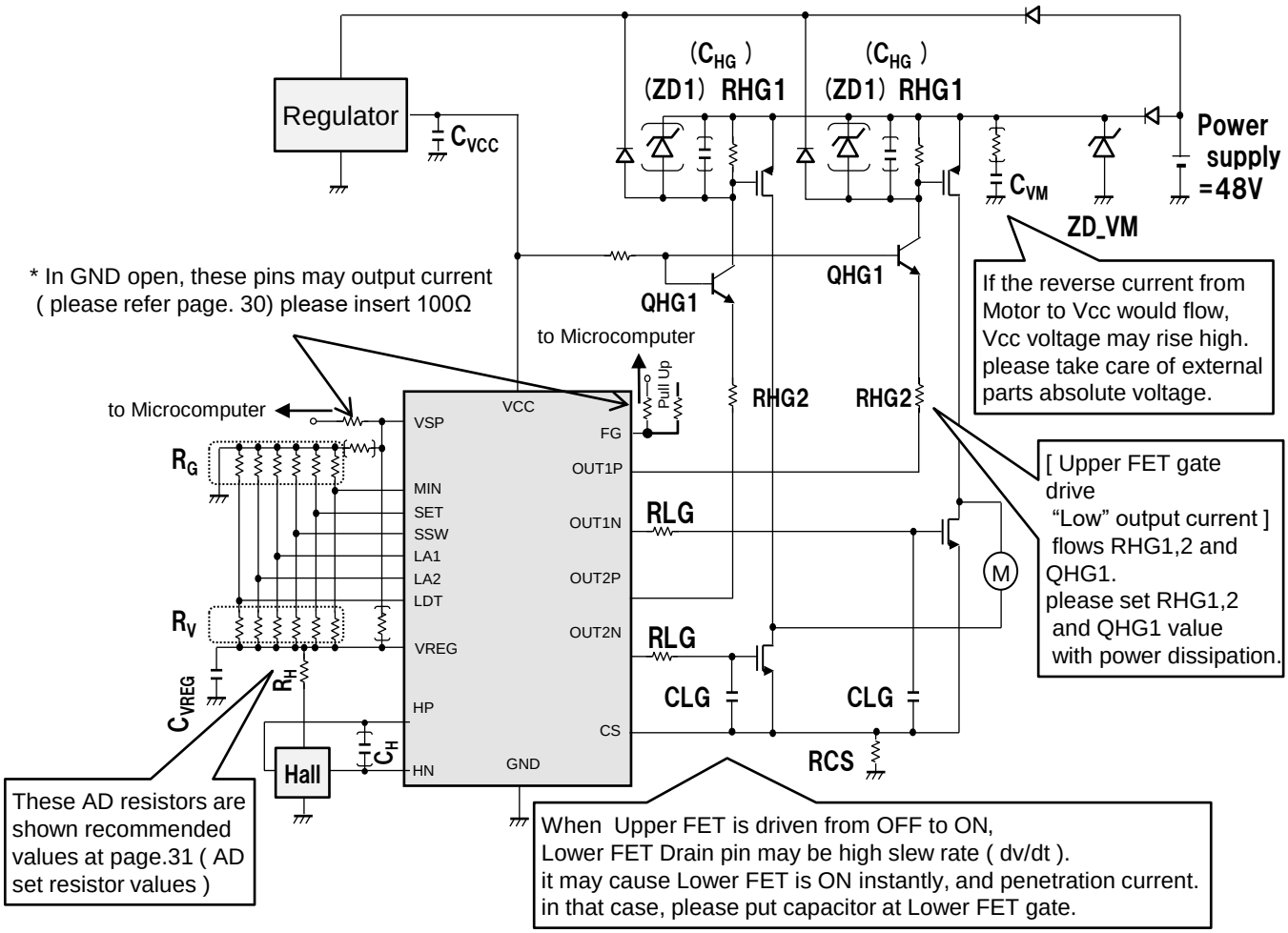


Note. The application circuit is an example. The operation of the mass production set is not guaranteed. Sufficient evaluation and verification is required in the design of the mass production set. The Customer is fully responsible for the incorporation of the above illustrated application circuit in the design of the equipment.

APPLICATION INFORMATION (continued)

1. Application information (continued)

■Application circuit 3



Note. The application circuit is an example. The operation of the mass production set is not guaranteed. Sufficient evaluation and verification is required in the design of the mass production set. The Customer is fully responsible for the incorporation of the above illustrated application circuit in the design of the equipment.

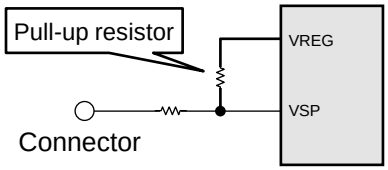
APPLICATION INFORMATION (continued)

2. VSP input block

Please add pull-up or pull-down resistor at VSP pin.
because if VSP connector is open, VSP is set Stop control or Max. speed drive.

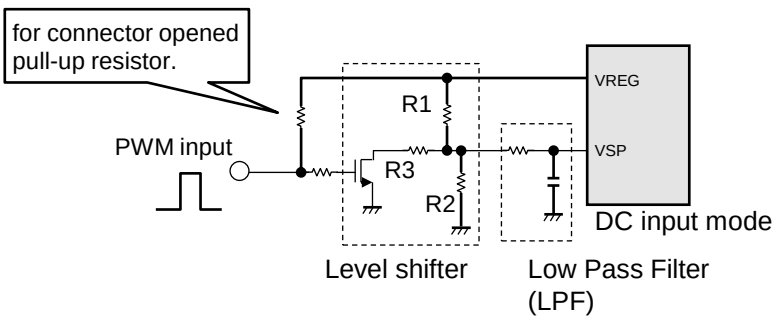
・PWM input mode
(a) Max. speed drive : Pull-up (100%duty)
(b) Stop control : Pull-down (0% duty)

・DC input mode
(a) Max. speed drive : Pull-down
(b) Stop control : Pull-up



・At below circuit,
PWM signal is changed input level by level shift circuit, and changed to DC signal by LPF.
so that, Stop control and Max speed drive input is adjusted.

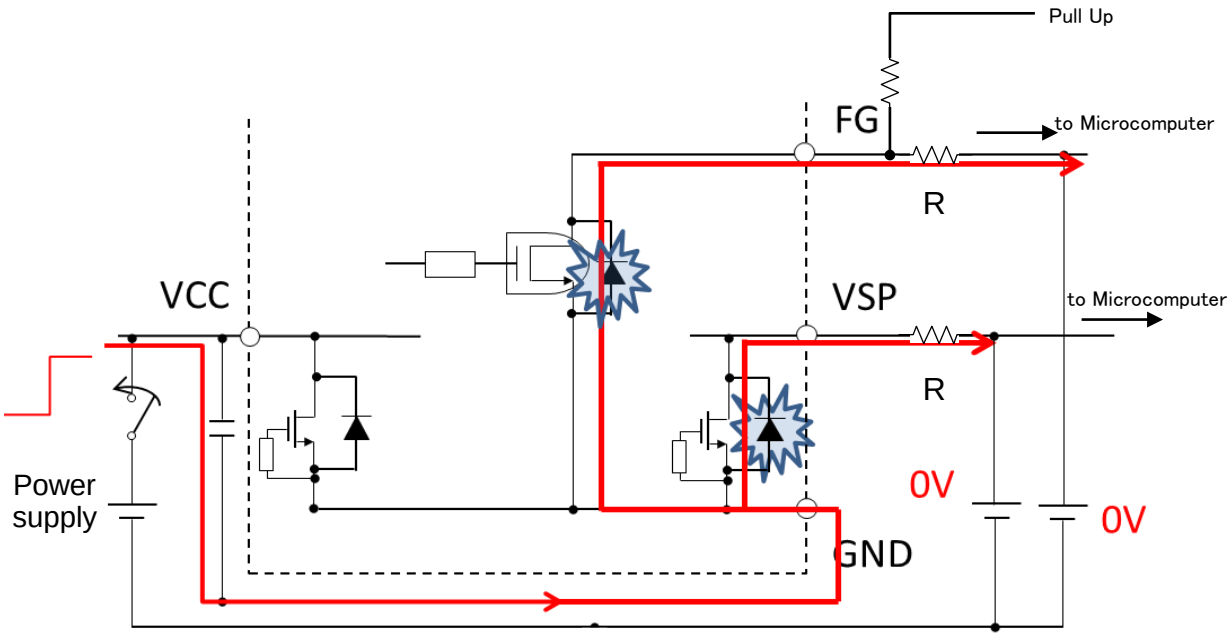
Fig. PWM input → DC input circuit



APPLICATION INFORMATION (continued)

3. Connection to Microcomputer

When Vcc is input with GND open, the current which is RED line at bellow figure flows.
this current are output from Vcc power to Microcomputer via FG and VSP pin.
it may cause that IC or Microcomputer are damaged.
please insert resistor (>100Ω) FG and VSP pin to prevent this current.



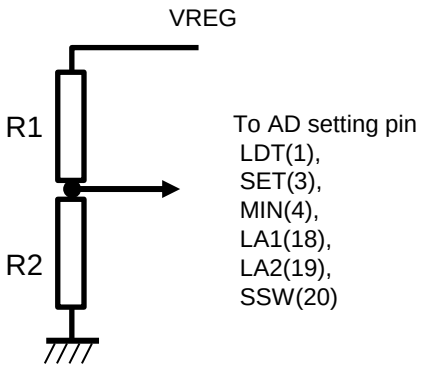
Vcc current course at GND open.

APPLICATION INFORMATION (continued)

4. Resistor value for AD setting.

The recommend resistor value for AD setting is shown at below table.
please use them for E24 preferred number and 1% tolerance.
the AD setting function is shown at AD control mode table (Page.12~14).

Definition of Resistor for AD setting.



E24 preferred number
1% tolerance

◆For LDT pin (1)

Setting Step	R1[kΩ]	R2[kΩ]
30,31	0	open
28,29	8.2	82
26,27	9.1	51
24,25	13	47
22,23	20	51
20,21	27	51
18,19	27	39
16,17	24	27
14,15	30	27
12,13	56	39
10,11	51	27
8,9	51	20
6,7	39	11
4,5	82	15
2,3	96.6 (91+5.6)	10
0,1	open	0

◆For MIN端子(4)
at setting step 0-1,16-17

Setting Step	R1[kΩ]	R2[kΩ]
16,17	24	27
0,1	open	0

For MIN pin,
the resistor value must be set
at above table to set step 0-1, 16-17.

◆For SET(3), MIN(4), LA1(18), LA2(19), SSW(20)

Setting Step	R1[kΩ]	R2[kΩ]
31	0	open
30	3.3	68
29	4.3	51
28	10	82
27	9.1	56
26	13	62
25	13	51
24	11	36
23	13	36
22	20	47
21	33	68
20	24	43
19	36	56
18	24	33
17	39	47
16	15	16
15	16	15
14	47	39
13	30	22
12	56	36
11	43	24
10	68	33
9	43	18
8	36	13
7	36	11
6	51	13
5	62	13
4	56	9.1
3	82	10
2	51	4.3
1	68	3.3
0	open	0

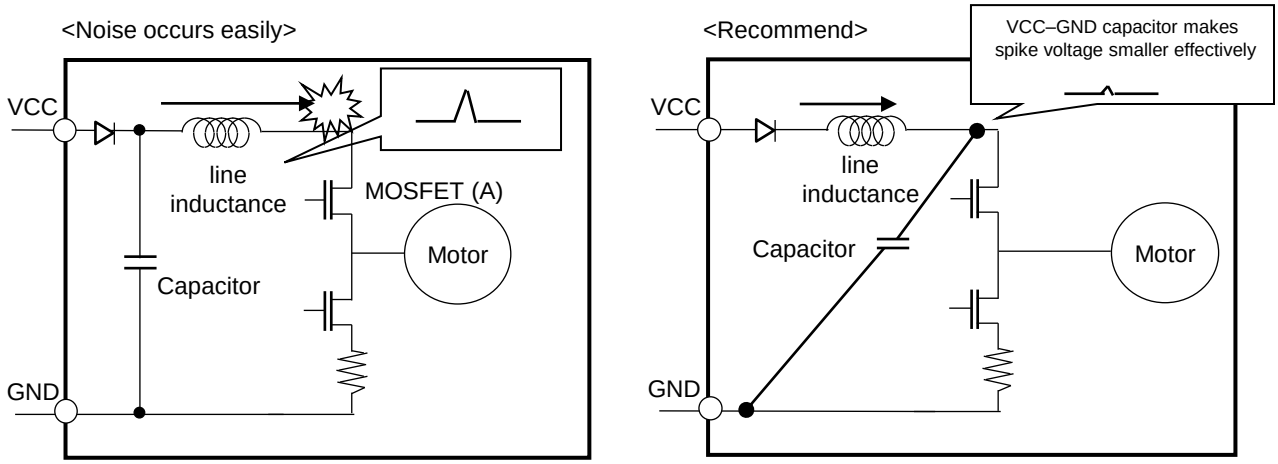
Note. The application circuit is an example. The operation of the mass production set is not guaranteed. Sufficient evaluation and verification is required in the design of the mass production set. The Customer is fully responsible for the incorporation of the above illustrated application circuit in the design of the equipment.

APPLICATION INFORMATION (continued)

5. Notes of layout

■VCC-GND Capacitor

This IC uses PWM driving. its noise may cause malfunction and circuit damaged by over voltage.
the note at below shows points of layout design.



At motor driving, Vcc current flows to MOSFET.
If Vcc line is long, this line has inductance.
even if MOSFET(A) is turn OFF, Vcc current is kept momentarily by this inductance.
it may cause over (spike) voltage at MOSFET, and damage IC or malfunction.

when the capacitor is put near MOSFET(A) (right figure shows), it makes spike voltage smaller effectively.

similarly, please put capacitor between IC Vcc pin and IC GND pin also.

APPLICATION INFORMATION (continued)

5. Notes of PCB layout

■CS lines

Motor current is detected by RCS resistor voltage.

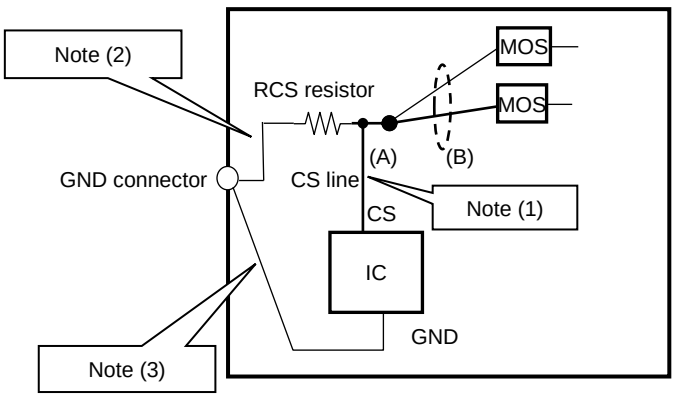
the voltage of RCS both pins need be detected for exact sensing. and one is GND pin, the other is CS pin.

Notes are shown at below.

(1) RCS resistor CS line is made independent from others.

(2) RCS resistor GND line is made as short and thick as possible.

(3) IC GND line is made independent from RCS line and other line which much current flow.

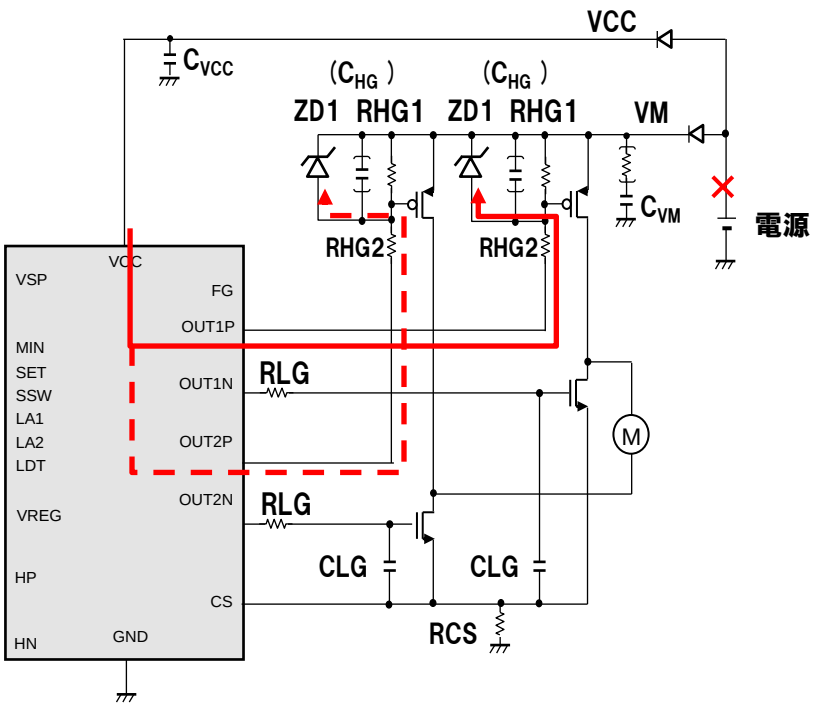


APPLICATION INFORMATION (continued)

5. Notes of PCB layout (continued)

■FET driving circuit

When Power supply is shut down during motor driving, Motor voltage (VM) may be less than IC Vcc voltage. then, Current flows from IC Vcc to VM via OUT1P (OUT2P), RHG2, ZD1.
please set RHG2 and ZD1 with power dissipation.



APPLICATION INFORMATION (continued)

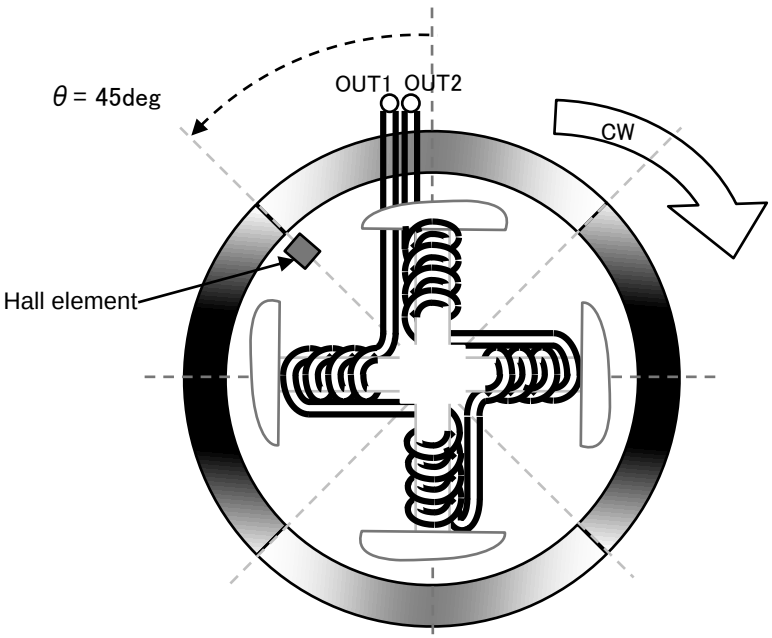
5. Notes of PCB layout (continued)

■Recommended position for hall element

This IC detects changing polarity of Hall signal (HP-HN) , and makes driving period. Soft switching and driving phase shift depend on the driving period.

it is recommended that the hall element is put in the position shown in the following figure.

Recommended position for hall element

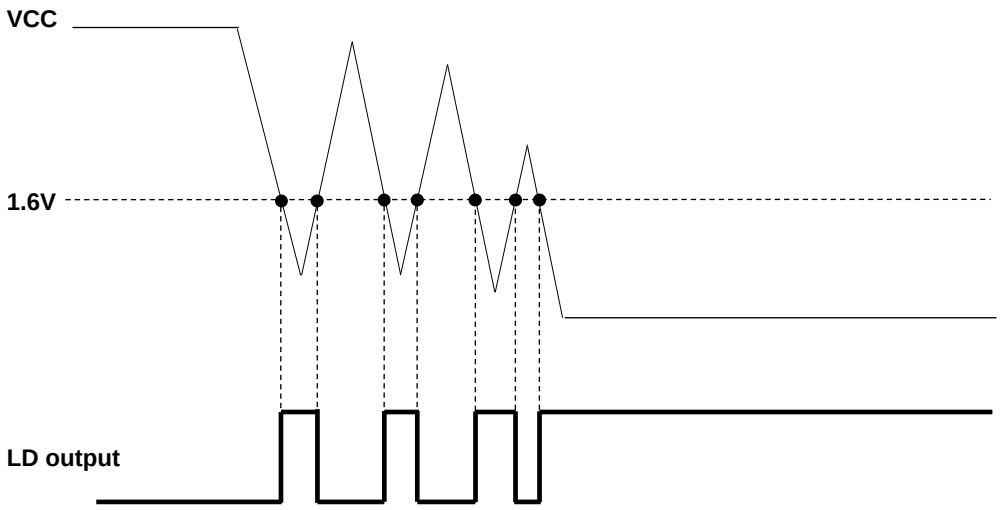


APPLICATION INFORMATION (continued)

6.Note at shut down

When Power supply is shut down during Motor driving, LD signal may get chattering.

After Vcc is shut down, Vcc voltage decreases with Motor rotating.
then, Vcc voltage is kept by BEMF voltage. and decreases with Motor slowdown.
When Vcc voltage is about 1.6V, LD gets chattering.
(because the internal circuit alternates of operating or not operating, because of Vcc voltage ripple.)



7.Start up from reverse rotation

Driving Motor during reverse revolution may cause Motor vibration, reverse current.

APPLICATION INFORMATION (continued)

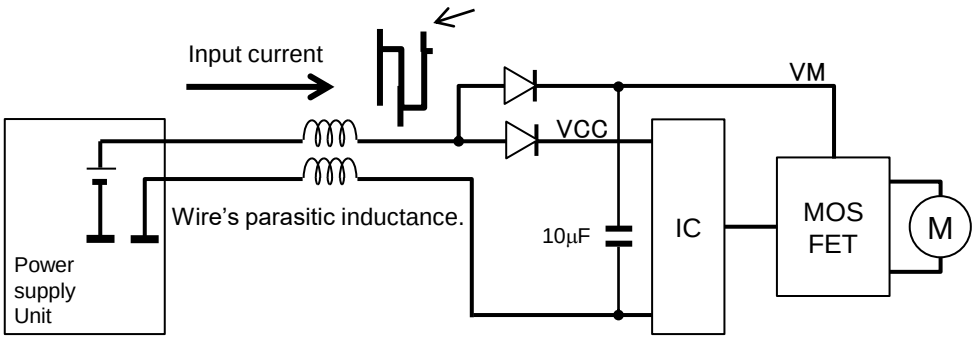
8. Precaution at PWM Motion

When VCC and GND wire is long, There is possibility which current peak of motor input current is caused at PWM motion due to wire's parasitic inductance.

Please countermeasure to reduce current peak of motor input current by adding a resistance in series with bypass capacitance and ensure sufficient evaluation is performed to verify that there is no problem.

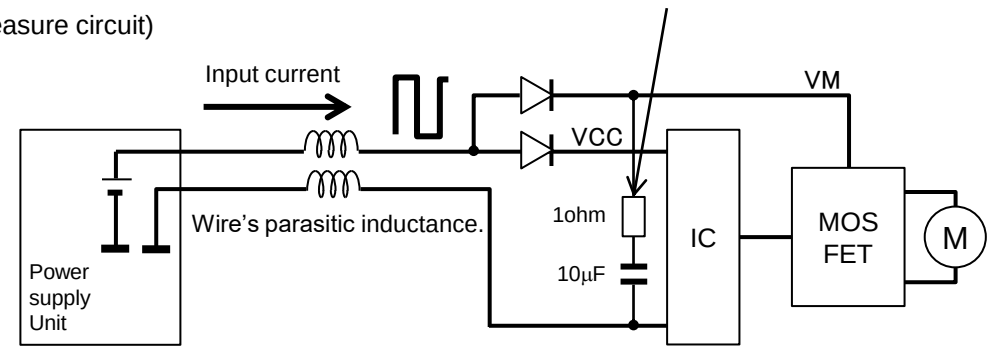
(Circuit)

The current peak is caused at PWM motion due to the wire's parasitic inductance.



The current peak is reduced according to adding in series with bypass capacitance.

(Countermeasure circuit)



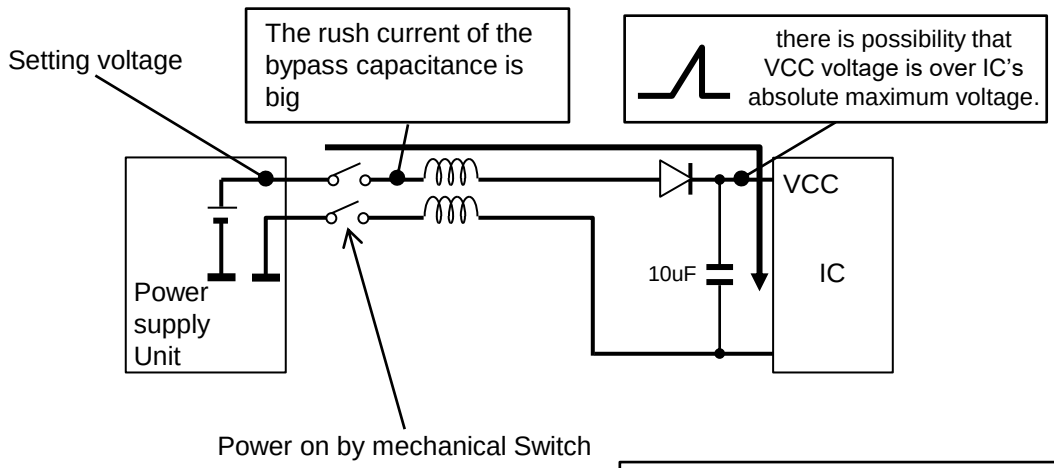
APPLICATION INFORMATION (continued)

9. Precaution at inputting power

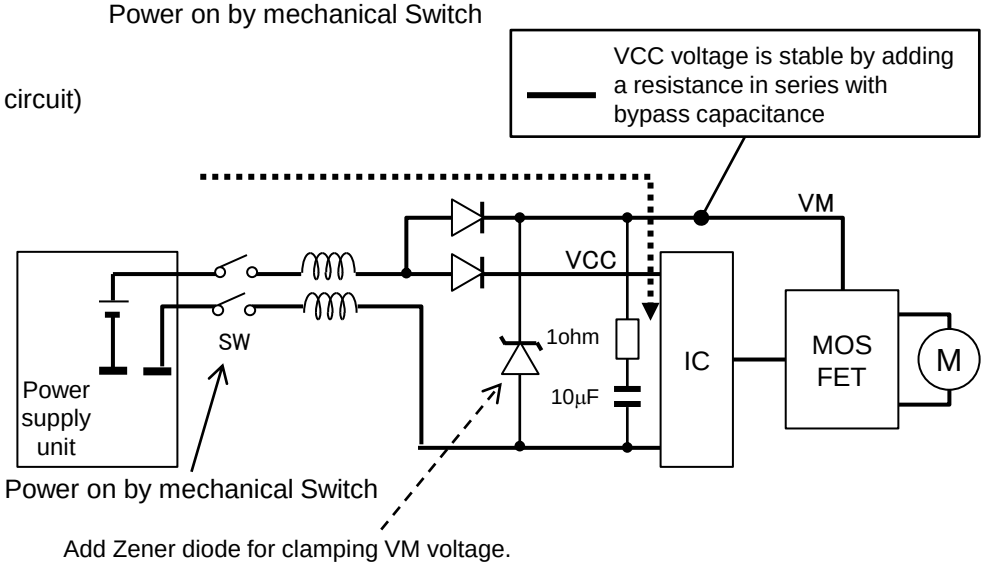
When the IC is powered on, it is recommended that VCC voltage rises slower than 0.24V/us, also when IC is shut down, it is recommended that VCC voltage falls higher than -0.24V/us, When power up is performed at high-speed, rush current must flow into bypass capacitance between VCC and GND. So VCC rises higher than setting voltage due to wire's parasitic inductance, there is possibility that VCC voltage is over IC's absolute maximum voltage.

in this case, please add Zener diode between VM and GND, to clamp Vcc voltage under absolute maximum voltage. and please countermeasure to reduce rush current by adding a resistance in series with bypass capacitance.
and ensure sufficient evaluation is performed to verify that there is no problem.

(Circuit) For example, in case of turning on the VCC by using the mechanical switch.



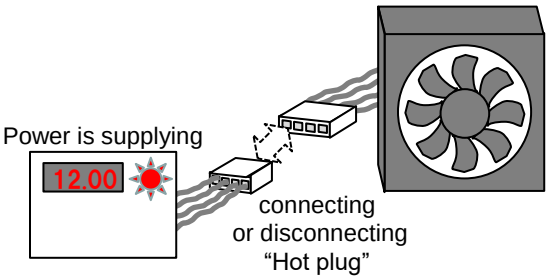
(Countermeasure circuit)

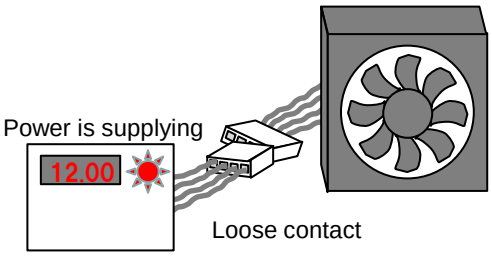


APPLICATION INFORMATION (continued)

10. Hot plug, Loose contact

During power supplying, when VCC, GND, I/F (VSP,FG etc.) pins get Hot plug, or loose contact. IC maybe supplied over voltage or current.



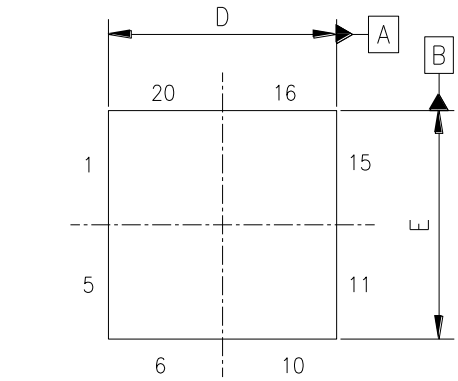


PACKAGE INFORMATION

Outline Drawing

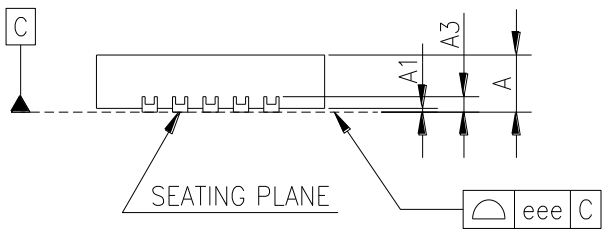
QFN 20L 3x3mm², Thickness 0.8mm, Lead Pitch 0.4mm,

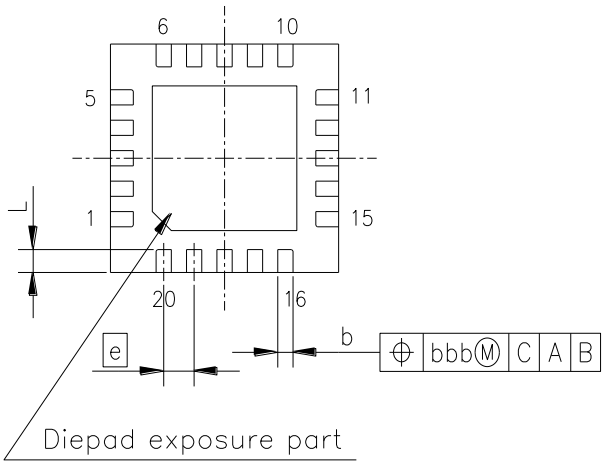
Lead Length 0.3mm, EP Size 1.9x1.9mm

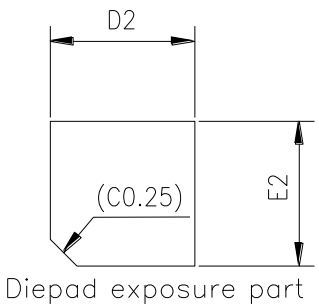


VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	–	0.05
A3		0.20REF	
D	2.90	3.00	3.10
E	2.90	3.00	3.10
b	0.15	0.20	0.25
bbb		0.07	
e		0.40BSC	
eee		0.08	
L	0.25	0.30	0.35
D2	1.80	1.90	2.00
E2	1.80	1.90	2.00







USAGE NOTES

1. Pay attention to the direction of the IC. When mounting it in the wrong direction onto the PCB (printed-circuit-board), it might be damaged.
2. Pay attention in the PCB (printed-circuit-board) pattern layout in order to prevent damage due to short circuit between pins. In addition, refer to the Pin Description for the pin configuration.
3. Perform visual inspection on the PCB before applying power, otherwise damage might happen due to problems such as solder-bridge between the pins of the IC. Also, perform full technical verification on the assembly quality, because the same damage possibly can happen due to conductive substances, such as solder ball, that adhere to the IC during transportation.
4. Take notice in the use of this IC that it might be damaged and be emitted a little smoke when an abnormal state occurs such as output pin-VCC short (Power supply fault), output pin-GND short (Ground fault), or output-to-output-pin short (load short). Safety measures such as installation of fuses are recommended because the extent of the above-mentioned damage will depend on the current capability of the power supply.
5. The protection circuit is for maintaining safety against abnormal operation.

   When sudden voltage or current change is applied to the pin, it may exceed the designated voltage and current level and therefore, customer shall perform sufficient evaluation and verification to ensure these are not exceeded in the usage.

   Especially for the thermal protection circuit, if the area of safe operation or the absolute maximum rating is momentarily exceeded due to output pin to VCC short (Power supply fault), or output pin to GND short (Ground fault), the IC might be damaged and emit smoke before the thermal protection circuit could operate.
6. Unless specified in the product specifications, make sure that negative voltage or excessive voltage are not applied to the pins because the IC might be damaged, which could happen due to negative voltage or excessive voltage generated during the ON and OFF timing when the inductive load of a motor coil or actuator coils of optical pick-up is being driven.
7. Product which has specified ASO (Area of Safe Operation) should be operated in ASO
8. Verify the risks which might be caused by the malfunctions of external components.
9. Connect the metallic plate (fin) on the back side of the IC to the GND potential. The thermal resistance and electrical characteristics are guaranteed only when the metallic plate (fin) is connected with the GND potential.
10. Comply with the instructions for use in order to prevent breakdown and characteristics change due to external factors (ESD, EOS, thermal stress and mechanical stress) at the time of handling, mounting or at customer's process.
11. Apply power supply with low impedance to VCC and connect bypass capacitor near to the IC.
12. Follow the power supply voltage, load and ambient temperature conditions to ensure that there is enough margin and the thermal design does not exceed the allowable value.
13. When designing your equipment, comply with the range of absolute maximum rating and the guaranteed operating conditions (operating power supply voltage and operating environment, etc.). Especially, please be careful not to exceed the range of absolute maximum rating on the transient state, such as power-on, power-off and mode switching. Otherwise, we will not be liable for any defect which may arise later in your equipment.

    Even when the products are used within the guaranteed values, take into the consideration of incidence of break down and failure mode, possible to occur to semiconductor products. Measures on the systems such as redundant design, arresting the spread of fire or preventing glitch are recommended in order to prevent physical injury, fire, social damage, for example, by using the products.
14. Pin 5(VSP) pins are MCU interface. In the case that the current setting of the motor is large and lead line of GND is long, the potential of GND pin of the IC may be increased.
    If 0V is input from the microcomputer, there is a case to be negative potential in the potential difference between the GND pin of this IC and the interface pin. If these pins detect under -0.3V, note that there is a possibility to break or malfunction.

Revision History

Date	Revision		Description	
2020.10.31	1.00	1	Initially issued.	
2022.01.28	1.05	1	Changed important notice	Page2
		2	Remove important notice page from previous version page42,43	-
		3	Added usage notes	Page43
		4	Change page number to refer because of adding page 2	Page2,6,9, 16-20,22,24,27-28,31
		5	PWM input frequency < 15kHz -> < 10kHz(TYP)	Page17
2022.8.31	1.06	1	Changed power dissipation rating notice	Page5
		2	Changed block diagram composition	Page11
		3	Deleted some Package information	Page41-42

Important Notice

Nuvoton Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, "Insecure Usage".

Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.

All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.